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Defining Switching Efficiency of Multilevel Resistive Memory with PdO as an Example

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Resistive random access memory (RRAM) is the most promising candidate for next generation nonvolatile memory. In this article, resistive switching in PdO thin film is investigated. The fabricated in-plane devices showed voltage pulse induced multilevel resistive switching (MRS) with as many as five states under ambient conditions with high degrees of retention and endurance. The *I–V* characteristics of the different memory states are linear and only a small reading voltage (≈10 mV) is necessary. Raman mapping of PdO (B_{1g} mode, 650 cm^{-1}) and temperature-dependent electrical transport measurements provide an insight into possible redox mechanism involving PdO/Pd particles. For the first time, the switching efficiency of a MRS device is uniquely defined in terms of a parameter called "multiplex number (*M*)," which is the sum of the total number of memory states and the ratio between the number of switching events observed in a device and the total number of possible switching events. The present PdO MRS device exhibits the highest *M* value compared to the values evaluated from the literature examples. Such high performance MRS in PdO devices makes them potential candidates for RRAM and neuromorphic circuit applications.

1. Introduction

Resistive random access memory (RRAM) as a next generation nonvolatile memory is promising because of the simple device geometry, ease of fabrication and operation.[1,2] In the recent past, multilevel resistive switching (MRS) for multiple memory states has gained much attention not only in the context of high density of information storage but also due to its relevance in neuromorphic circuitry.[3,4] While the overall size of the device may be similar to that of a binary device, the active material in it is expected to store multiple bits enhancing the storage capability by few orders with no extra burden on fabrication. Among numerous resistive switching (RS) materials,[5,6] metal oxides are preferred from the fabrication point of view and have been extensively studied.[7,8] Besides several RS devices with binary states,[9,10] there are examples of 3 or 4 resistive states[11–35] but only a few attempts have been made to achieve 5 or more states.[36–43] As the number of memory states (n) increases, the number of switching events in between the states increases which can be defined in terms of probability as ${}^{n}P_{2}$. In practice it is rather challenging to achieve all switching events reliably over many cycles. With binary memory, high degree of endurance is commonly achieved.[9] For a MRS device with three states, the possible switching events are six and only one example[15] is found in the literature showing all possible switching events, while in another example[18] the switching possibility was only partial. Four-bit MRS devices have 12 switching events out of which 10 events have been successfully demonstrated.[27] In a study by Huang et al. on a 5-state device,[41] nearly half of the total 20 switching events were attempted. Recently, Zhao et al. fabricated a MRS device with as many as eight states, but switching was possible only in between the neighboring states.[44] However, if the advantage offered by multilevel memory is to be effectively utilized, switching between any combination of resistive states should be facile with no room for failure. Surprisingly, there is very little discussion in the literature on measurement or quantification of the efficiency of a MRS device to randomly switch between all possible states. Thus far, most MRS devices reported have not considered switching events other than, from and to the "0" state. Ideally, a MRS device should host a large number of memory states and should allow all possible switching combinations.

A resistive memory device works based on the principle of filament formation and oxygen vacancy migration, etc. Oxides as dielectric materials become leaky beyond a critical electric field, which along with other parameters decides the resistance of the "leaky" (memory) state. Unlike binary devices, MRS devices require relatively well defined resistive states, a prerequisite for controllable switching between the states. Many oxides and oxide containing hybrids have been tried out in this context. Simple oxides such as NiO,[45] SiO_2,[46] ZnO,[47] HfO_x[48]

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have shown promising resistive switching but the number of resistive states are usually limited. The fabrication of a MRS device using metal oxide relies on the ability in precisely controlling the oxygen vacancy migration and the formation of conducting filaments which in turn, demand a clear insight into the switching mechanism. Such stringent requirements have prompted researchers to look out for new materials for resistive switching. Toward this end, multilayered NiO/Pt nanowire arrays have been fabricated in which five resistive states could be realized.[41] In this case, the fabrication required sophistication and the switching was possible only in between the neighboring states. Recently, a three-layer vertical $AlO_{\delta}/Ta_2O_{5-x}/TaO_y$ stack has been formulated to achieve a 3D MRS device,[49] but it involved laborious lithography processes for fabrication.

Here, we have chosen palladium oxide (PdO) as a novel active element for RS because of multiple redox states achievable in the Pd-O system.[50] The devices configured in planar geometry have been explored for the multilevel resistive switching and five distinct memory states have been achieved with well-defined reset voltage pulses. Further, a detailed insight was obtained on the switching mechanism by employing Raman spectroscopy and low temperature resistance measurements. For the first time, an effort has been made to examine all the possible switching events. We have defined a new parameter called as "multiplex number," to quantify the number of possible switching events for a MRS device. The present PdO device is found to exhibit the highest multiplex number.

2. Results and Discussion

The first few steps in device fabrication involve synthesis of PdO film on a mica substrate as shown in the schematic of **Figure 1**a. Pd hexadecylthiolate was drop-coated on the substrate to form yellowish colored film which was thermalized at 600 °C in oxygen. As the organic components were removed, the film turned to brownish black marking the formation of PdO. The X-ray diffraction (XRD) pattern in Figure 1b shows the presence of nanocrystalline tetragonal phase of PdO which is indexed with JCPDS No. 431024. The scanning electron microscopy (SEM) image in the inset of Figure 1b shows particles of size 20–40 nm well packed into a continuous film of measured thickness ≈60 nm. An optical band gap of ≈1.7 eV was estimated from the UV–vis absorption data (Figure 1c and see Supporting Information, Figure S1), which may be compared with the literature value of ≈2 eV for PdO.[51] The PdO thin film is ≈40% transparent at 550 nm (see Supporting Information, Figure S1). This is also evident from the photograph shown in the inset of Figure 1c, where the letters behind the PdO film are clearly seen.

A planer resistive switching device was fabricated by depositing Au metal electrodes on top of a PdO film by shadow masking a gap of ≈7 μm (see inset in **Figure 2**a) across the entire length (3 mm) of the film. To initiate resistive switching, the device was taken through a forming process (Figure 2a) by varying the applied voltage in ambient conditions. As the voltage was increased from 0 to 7 V, the current increased sublinearly before showing a breakdown around 6 V. This is a forming step in which a conducting pristine device (≈100 Ω) is taken to a less conducting state (≈2 kΩ) irreversibly. In the RESET process, a 0 to 10 V voltage sweep was performed (see black curve) as shown in Figure 2b. The device showed a linear increase in current up to ≈5 V, beyond which it saturated and became unsteady. The dotted line indicates the resistance state of the device (also see Supporting Information, Figure S2), which was read out with a 0 to 1 V sweep (blue curve) and

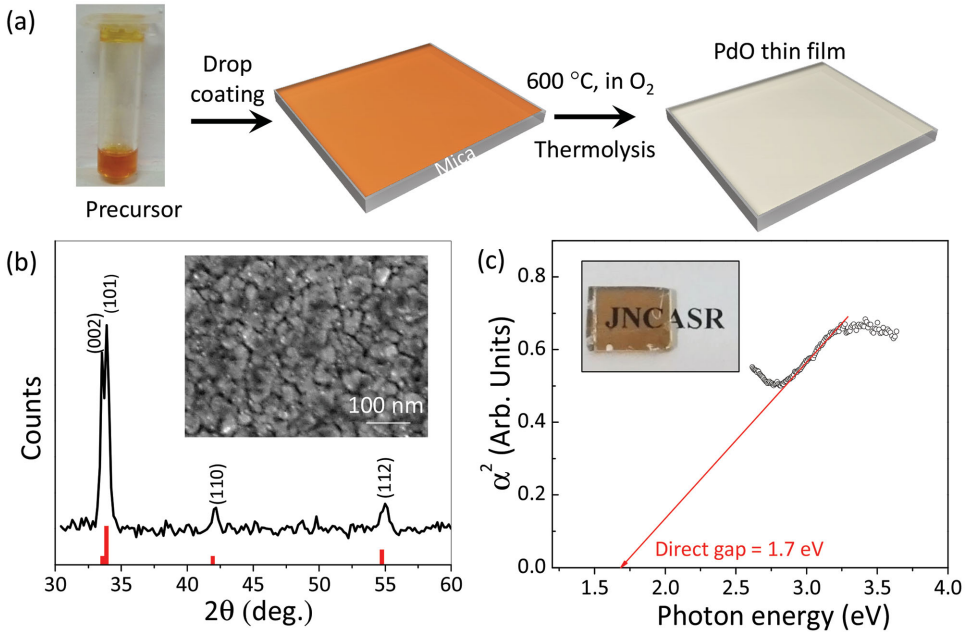

Figure 1. a) Schematic illustration of the synthesis of PdO thin film. Characterization of PdO thin film, b) XRD pattern indexed with JCPDS file number-431024, where standard peaks have been marked in red. Inset shows a typical SEM morphology. c) Variation in absorption coefficient with photon energy. Inset shows the photograph of the PdO thin film.

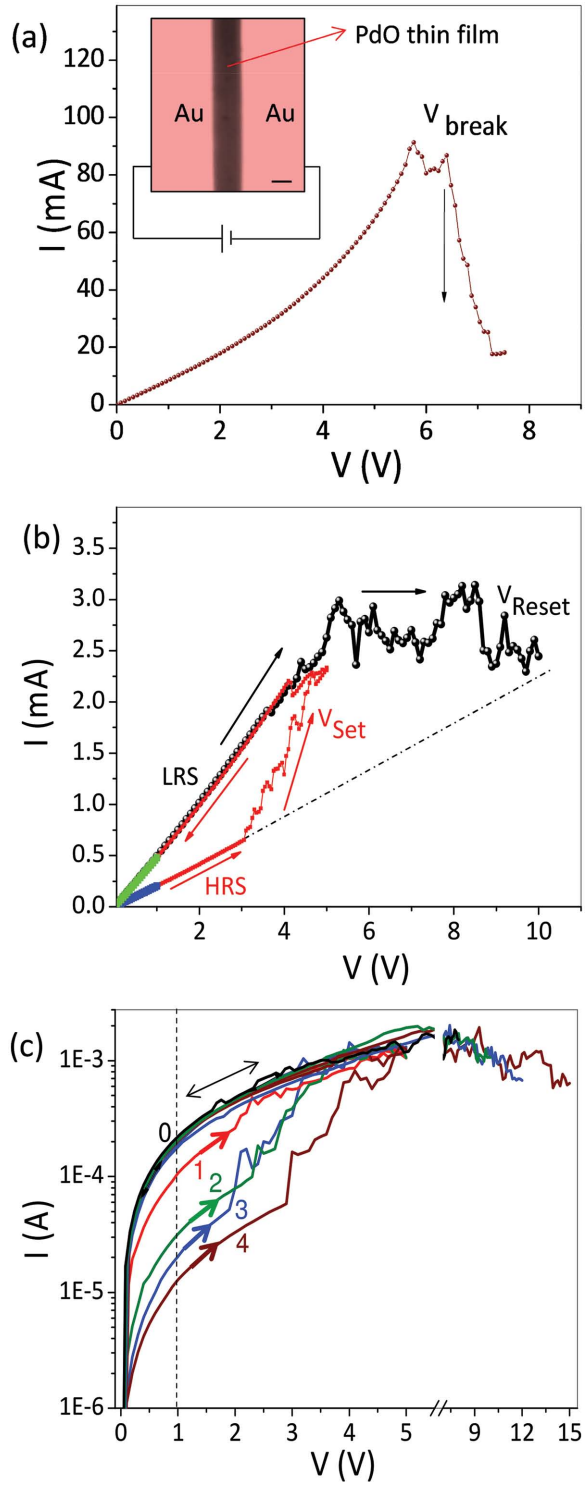

Figure 2. a) *I–V* characteristics of the voltage-controlled forming process, optical image of PdO thin film device along with in-plane Au electrodes (scale bar 5 μm). b) Typical switching characteristics of the device. LRS, the low resistance state and HRS, high resistance state are marked. Blue and green lines near origin refer to reading of the respective state. c) Consecutive voltage cycling from 0 to 5 V (arrows indicate the direction of voltage sweeps). Following RESET voltage sweeps 8 V (red), 10 V (green), 12 V (blue), and 15 V (brown) and each RESET process is followed by a SET process by applying a 0–5 V cycle. Arrows indicate the direction of sweep.

this value is assigned as a high resistance state (HRS). In the following voltage cycle, 0 to 5 to 0 V, the curve (red) trailed HRS up to ≈3.6 V, beyond which it became unsteady only to increase and settle in a low resistance state (LRS) at ≈5 V. This state of the device was again measured by a sweep, from 0 to 1 V (green). Thus, two resistance states, namely, LRS and HRS were defined for the fabricated PdO device with V_{RESET} (LRS to HRS) and V_{SET} (HRS to LRS) at ≈10 and 5 V, respectively and with V_{Read} of <1 V. Likewise, we could activate several devices (see Supporting Information, Table S1). From these measurements, it is evident that PdO can potentially be used to define resistive memory states. In order to explore possible presence of multiple resistive states, higher V_{RESET} voltages were tried out with another device (Figure 2c). Beginning with the LRS ("0") state, four high resistance states (HRSs, red curve, "1", green, "2", blue, "3" and brown, "4") were observed in sweeps with applied bias voltages of 8, 10, 12, and 15 V, respectively. Beyond 15 V, the device became unstable. Importantly, the device was retrieved back to the "0" state by cycling the voltage from 0–5 V. Note-1 in the Supporting Information provides the details of the voltage sweep/cycles. The voltage cycling was also tried out to switch the device in-between the states as depicted in Figure S3 of the Supporting Information.

The switching between MRSs could also be achieved by applying a voltage pulses instead of voltage sweeps. In this approach, a set of increasingly higher voltage pulses, 5, 8, 10, 12, 15 V, were applied successively to the PdO device each for 20 ms (**Figure 3**a, top panel) while the resistance being read in between by a readout voltage of 10 mV (see bottom panel). The detailed information regarding voltage pulsing is provided in the Supporting Information, Note-2. Thus, it was possible to switch steadily from the "0" state to any one of the four ("1", "2", "3", and "4") states and vice-versa with the predetermined voltages. In this way, several devices were initiated into MRS (see Supporting Information, Figure S2), emphasising the versatile and consistent nature of PdO for memory device applications. These designated states are persistent and well defined, as evident from Figure 3b, where each state was monitored in the ambient for 10^3 s using 10 mV reading voltage. The resistance variation was less than 3%, 0.5%, 0.9%, 1%, and 1.7%, respectively, for the "0" to "4" states, demonstrating high stability of the PdO MRS device. Further, in the retention test performed over 25 cycles (see Figure 3c), the device showed a consistent, reliable and controllable multilevel resistive switching.

In order to understand the electrical nature of the memory states, temperature dependent resistivity measurements were carried out while the device was held in different memory states (**Figure 4**a). In each state, the resistivity was found to increase with decreasing temperature revealing a semiconducting nature. Generally, metallic conduction has been observed in many resistive switching materials such as in HfO_2[19] and CuO_x[37] with metallic species resulting from oxide reduction forming filamentous paths in the insulating matrix. The resistivity data (Figure 4a) was fitted with variable range hopping (VRH) equation

$$R(T) = R_0 \exp[(T_0/T)^a] \quad (1)$$

$$E_a = K_B T \quad (2)$$

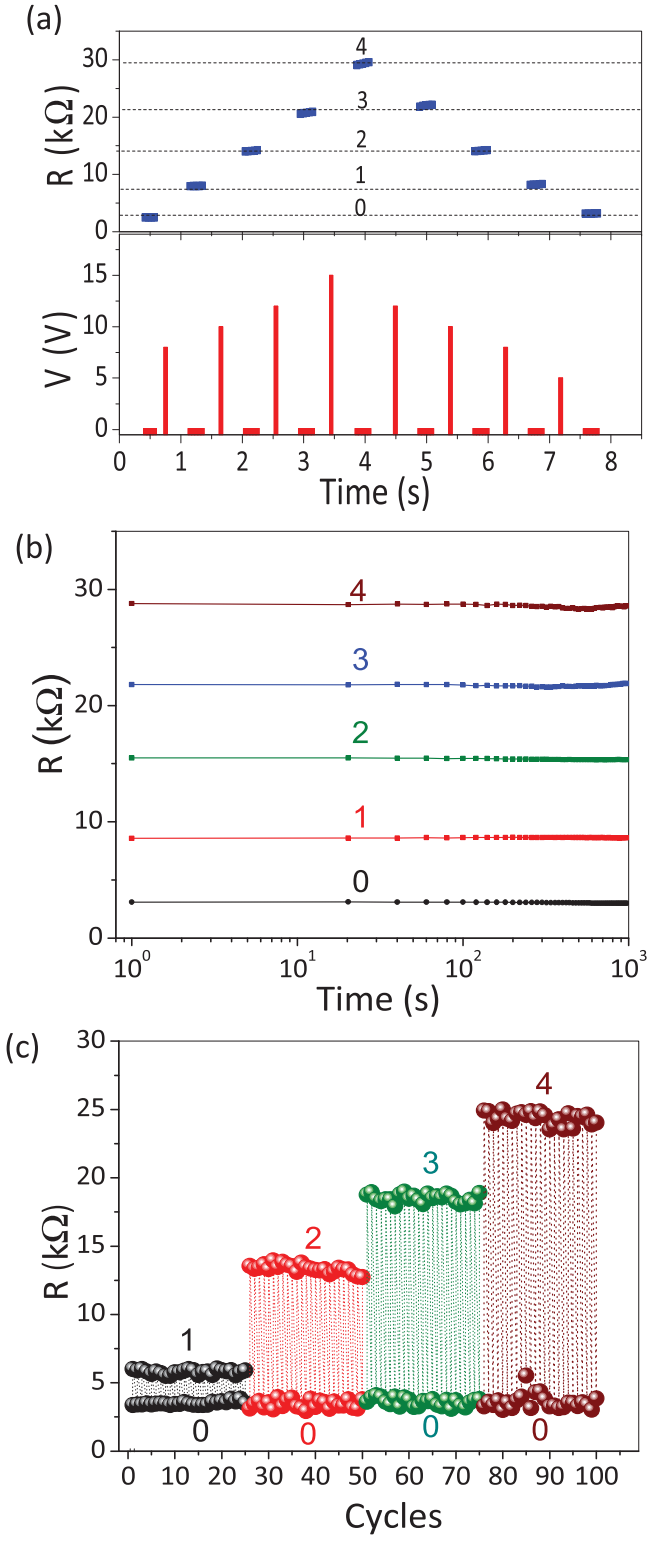

Figure 3. Electrical characteristics of the PdO MRS device: a) Top panel, resistance states achieved with different RESET voltage pulses 5, 8, 10, 12, and 15 V (pulse duration 20 ms) and bottom panel, resistance read out using a reading voltage 10 mV (pulse duration 20 ms, each memory state was read for 10 times). In bottom panel, the RESET voltage time scales are magnified (×5) and reading voltage scales are magnified (×100) for better visibility. b) Retention and c) endurance of the MRS device.

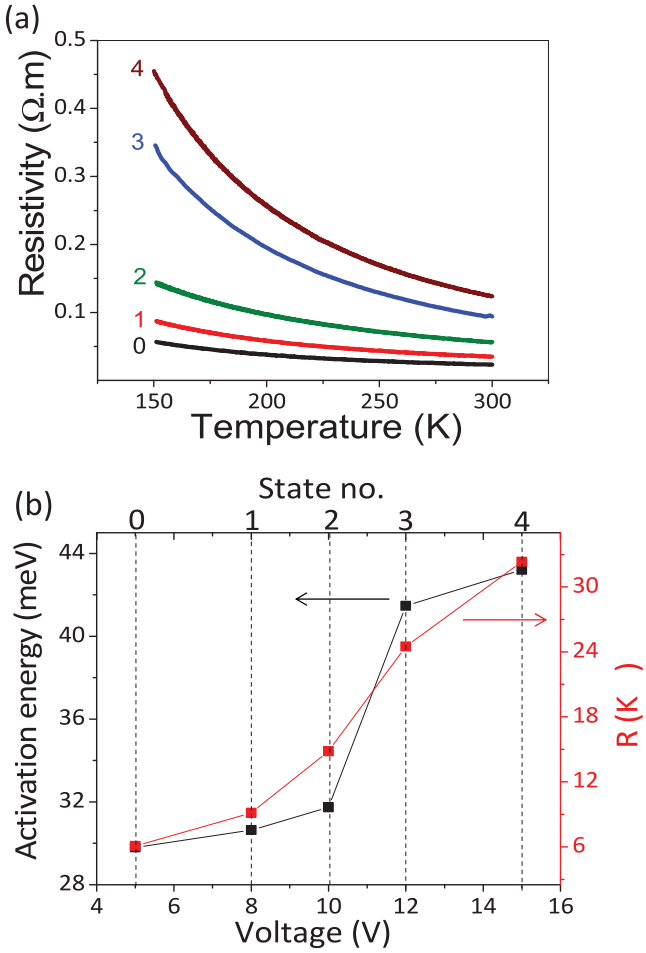

Figure 4. a) Resistivity measurements of all five resistive memory states from 150 to 300 K. b) A plot between estimated activation energy from VRH model and REST voltage and room temperature resistance for each memory state.

where $R(T)$ is temperature dependent resistance, R_0 is temperature independent prefactor, T_0 is characteristic temperature, a is exponent, E_a is activation energy, and K_B is Boltzmann constant. The best fit for the low temperature data was obtained with $a = 1/3$, indicating a 2D VRH type conduction in the nanocrystalline thin film.[52] The estimated activation energy (using Equation (2)) values from the VRH model, the room temperature resistance and the corresponding V_{RESET} values are shown in Figure 4b in the form of a plot against the designated memory states. The activation energy is seen to increase with the state complementing the variation in resistance, indicating an increase in the barrier height for the charge carriers. It remains to be seen what is responsible for this activated behavior in different resistive states.

This novel behavior of PdO MRS device deserves careful microscopy analysis (**Figure 5**). Following the forming step, SEM imaging revealed a crack of width 1–3 μm in the PdO film (Figure 5a,b) near the centre of the gap electrodes along the entire length (≈3 mm), while the regions close to the electrodes remained unchanged (marked as "c" in Figure 5b). Such crack formation has been commonly observed in metal

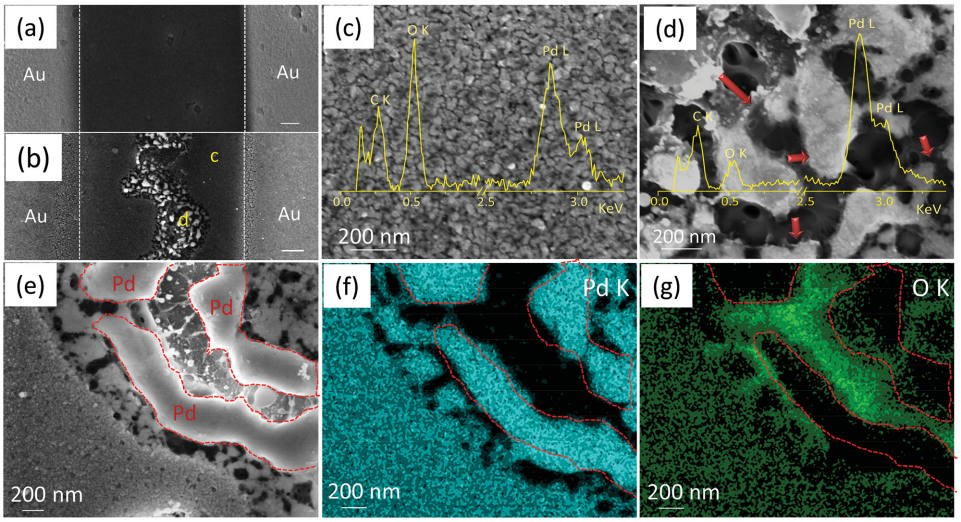

Figure 5. Microscopy analysis of the device active area, a) before and b) after forming, c) outside and d) in the cracked regions. The magnified images only with EDS spectra from these regions are shown along side. The arrows in (d) point to Pd nanoparticles in the intervening regions connecting larger Pd islands. An interface region shown in e) SEM image with corresponding f) Pd K and g) O K EDS maps.

oxide based resistive switching devices.[4,36] The magnified view of the crack region "d" in Figure 5b shows random distribution of particle agglomerates in the range 0.2–2.5 μm (Figure 5d). What is noteworthy from the Energy-dispersive X-ray spectroscopy (EDS) analysis (Figure 5c,d) is that significant differences exist the two regions particularly in respect to the oxygen signal. The agglomerates (colored white) in region "d" show the predominant presence of Pd with very little oxygen. This is clearer in EDS mapping shown in Figure 5f,g corresponding to the magnified portion of the PdO-crack in Figure 5e. In the forming process due to large current through the PdO thin film, joule heating is expected which can locally convert PdO to Pd, provided favourable temperature (≈700 °C) is achieved.[53,54] As heat dissipation is relatively less in the gap region unlike the regions nearer to Au electrodes, where heat dissipates easily due to high thermal conductivity of Au, a thermal gradient is expected across the gap.[55] Thus, the reduction process is restricted to the centre of the gap region of the PdO film. After the forming process, Pd/PdO nanoparticles tend to occupy the space between large Pd particles (see Figure 5b for cracked region which is magnified in (d)) which aid the formation of percolation networks responsible for conduction. Even larger Pd islands can thus participate in transport due to increased interconnectivity bringing down the resistance to few kilo Ohms. Once formed, the changes are only local. A higher voltage sweep can now produce enough Joule heat to cause oxidation of particles in the cracked regions.

In order to gain further insight into the spatial distribution of Pd and PdO species, Raman mapping was carried out across the crack region while the device was maintained in different memory states, as shown in the schematic in **Figure 6**a. The PdO film outside of the crack gap region exhibited a Raman peak at 650 cm^{-1} corresponding to a B_{1g} mode in PdO (Figure 6b).[56] Raman maps with respect to this feature were collected over a 6 × 6 μm^2 area in the crack region after applying successively programming voltages of 5, 8, 10, 12, and 15 V (Figure 6c–g). The black patches in the maps correspond to the presence of Raman inactive Pd regions while blue represents the presence of PdO. With increasing V_{RESET} (from "0" to "4"), the blue region increased gradually as evident from Figure 6h. As a result, the crack appears to be closing in (see Figure 6c–g). This may be attributed to the surface oxidation of Pd to form PdO nanoparticles. Some particle movement arising from electromigration is noticeable, which is quite common among the RS devices.[57] When the device was tried out in Ar atmosphere, no controlled switching was observed, while in neat oxygen, achieving low resistance state proved difficult due to excessive oxidation during RESET process (see Supporting Information, Figure S5). It is interesting to note that atmospheric oxygen works well for the device, unlike RS switching materials such as SiO_2/graphene, which require vacuum for reliable switching.[36] Moreover, the present PdO-Pd device works equally well with positive and negative voltages (see Supporting Information, Figure S6) and is, therefore, essentially a nonpolar device.

From the observations made from Figures 5 and 6, it is evident that resistive switching in our device occurs due to the versatile nature of the PdO/Pd/PdO conversion in the conduction path, Au pad-PdO film-PdO/Pd/PdO filament-PdO film-Au pad. In the forming process, PdO film cracks and filamentous agglomerates made of reduced Pd appear in the region giving rise to a low resistance state identified as "0" memory state. In the RESET process, Pd particles are gradually oxidized[50,58] which accounts for the increase in the resistance. Interestingly, it is well known in the literature that the oxidation of Pd particles has been accomplished by four oxidation stages i.e., chemisorption, surface oxidation, subsurface oxidation, and bulk oxidation. The oxidation of Pd particles is gradually increasing with each stage. In the present scenario, the oxidation stages were attained by applying increasing V_{RESET}, leading to four distinct high resistance memory states. In the SET process, joule heating reduces PdO particles to Pd. PdO is known to convert to Pd at elevated temperatures.[54] Electromigration may also play a role in MRS. The mechanism of PdO MRS

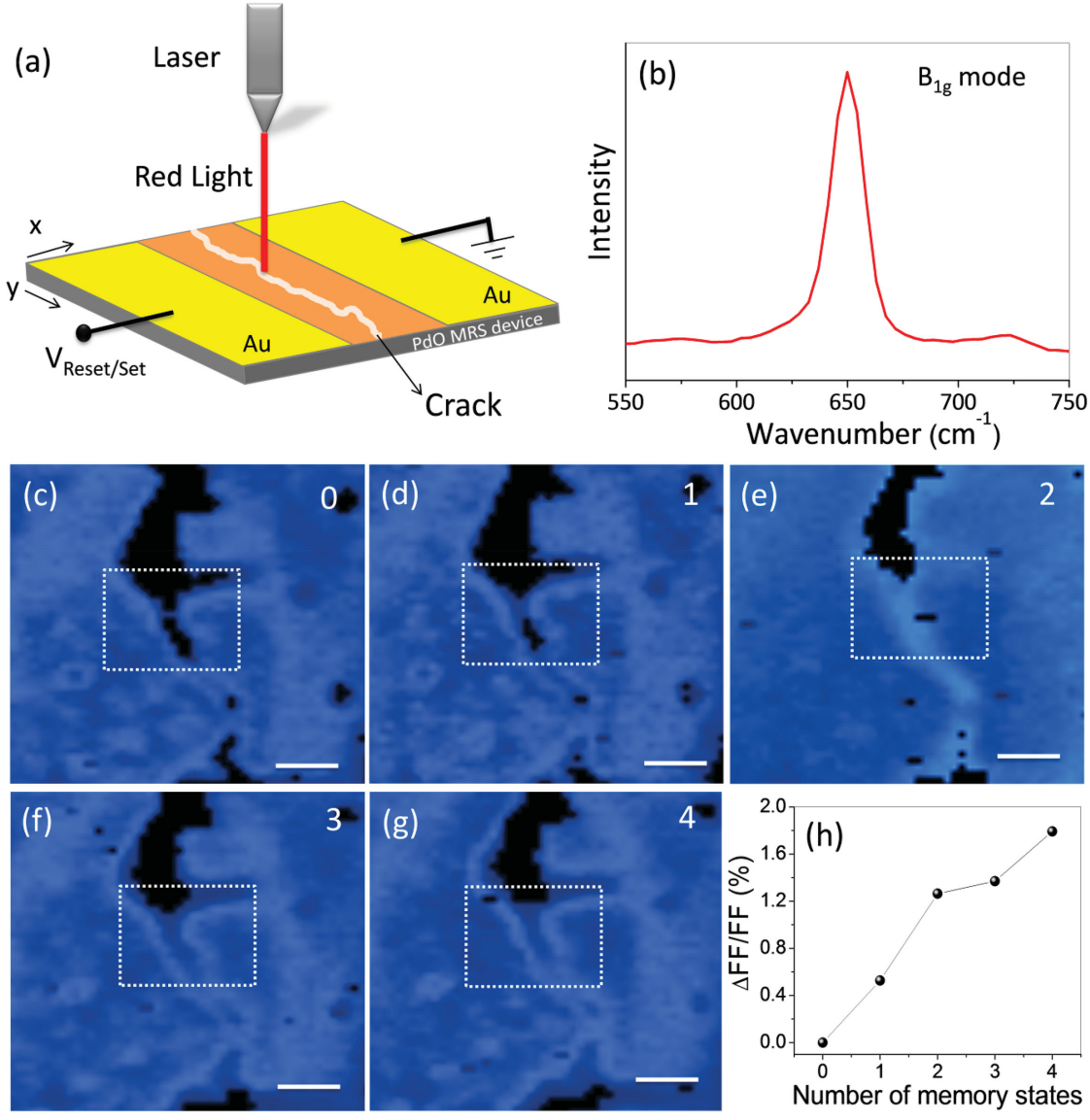

Figure 6. a) Schematic illustration of the Raman spectroscopy measurements of an active MRS device. b) Raman spectrum of the PdO thin film, showing B_{1g} mode. c–g) Raman mapping of PdO signal near cracked region after applying 5, 8, 10, 12, and 15 V, respectively, to achieve the different resistance states (scale bar 400 nm). The number at the top right corner represents memory state. The rectangular box represents the active area of the device. Blue and black regions stand for the presence and absence of the PdO signal, respectively. h) Relative change in the PdO fill factor against the memory states, estimated from images in (c) to (g).

device is schematically shown in Figure S7 of the Supporting Information. In the RESET process, the power consumed (less resistance and more voltage) is more as compared to the SET process (more resistance and less voltage). Therefore, power applied in the RESET causes higher joule heating leading to oxidative condition whereas in the SET process, lower power consumed may generate relatively lower temperature suitable for reduction of Pd/PdO nanoparticles. Thus, controlled and reversible surface oxidation/reduction of the active Pd nanoparticles present in the crack region enables RS in PdO MRS device.

In the literature, the intermediate state switching of multistate memory devices is hardly discussed. The switching events are reported typically from and to the "0" state. In this study, we have paid more attention to intermediate state switching and have therefore examined the device carefully for its reliability for random switching. In the present PdO MRS device with five memory states, maximum possible switching events are 20, out of which only 14 could be fully (probability, 100%) realized (**Figure 7**a), which are shown as black bars in a probability histogram in Figure 7b. These are the events involving two neighboring states and also those well separated but involving "0" as one of the states. When the participating states are well separated and not involving "0" (see red bars), the switching probability is in the range of 15%–60% (also see Supporting Information, Figure S8). Finite probabilities of interstate

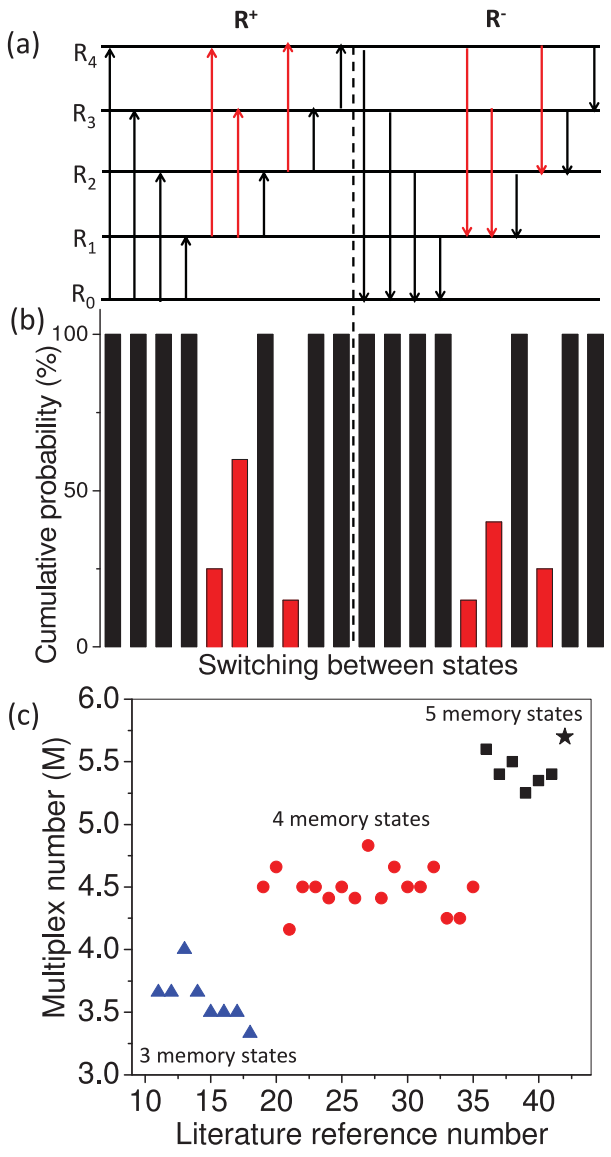

Figure 7. a) Schematic illustration of switching between the memory states. Fully possible and partially possible switching combinations are represented with black and red arrows, respectively and b) histograms of the corresponding cumulative probabilities for all switching combinations. c) The multiplex number and number of memory states for various MRS devices fabricated in the literature.[11–42] "Star" represents the present study.

switching may arise due to lack of control over Pd/PdO partial oxidation/reduction processes, particularly while dealing with intermediate interstate switching. A better control of the processes is possible when state "0" is involved or between two neighbor states. Interestingly, the more the separation between the states, lesser is the switching probability, when state "0" is not involved in switching events.

To the best of our knowledge, there has been no effort in the literature toward evaluating a MRS device, or for that matter any memory device, in terms of its switching efficacy or a figure of merit. For the first time, we define a new parameter which we term as "multiplex number (M)" to quantify the performance of a multiple memory switching device. It is defined as

$$M = n + \{\gamma/({}^{n}P_2)\} = n + \{\gamma/(n!/(n-2)!)\} \quad (3)$$

here n is the number of states, and γ is the number of fully possible switching events in between the memory states, and ${}^{n}P_2$ is the number of possible combinations of switching events in between the memory states. The first term enunciates the number of memory states in a device and the second term quantifies the fraction of switching events fully possible as against the total number; ideally, the second term should be unity. In other words, a MRS device with n states should have M of $n + 1$, but in real situations, the M value stands between n and $n + 1$. It should be noted that M stands for a unique situation. In the present PdO MRS device, the multiplex number is 5.7, which may be interpreted as five memory states with an overall 70% efficiency in switching. If it were to work with full efficiency M would be 6.0. Interestingly, M of 6.0 cannot represent a six state device as its efficiency would be reduced to zero! Similarly for all binary devices, M value will be 3 as switching efficiency ("0" to "1" and "1" to "0") is always 100%. An M value of 5.7 for the present device is the highest value estimated, compared to other MRS devices reported in literature[11–42] (Figure 7c and Supporting Information, Table S2).

3. Conclusions

In this study, nanocrystalline PdO thin film has been successfully demonstrated as a MRS element working in ambient conditions. The PdO MRS device has shown as many as five resistive memory states. The memory states are quite stable with high endurance and retention with variation less than 3%. The reading of the resistance states could be done with just 10 mV, due to linear nature of the I–V characteristics. Based on low temperature resistance measurements, the conduction mechanism in the resistive memory states was found to be variable range hopping (VRH) with the activation energy increasing with increasing resistance of the memory state. SEM imaging and EDS mapping have shown crack formation in the oxide film and reduced Pd agglomerate formation. Raman mapping showed that the crack closes due to the surface oxidation of Pd to form PdO nanoparticles involving electromigration of nanoparticles to some extent. The reversible oxidation/reduction of the active Pd/PdO particles is the basis of the observed MRS. For the first time, a "multiplex number" has been defined to quantify the switching efficiency in-between the memory states. Importantly, this approach can be generalised to any type of memory device. The multiplex number for the present PdO MRS device is 5.7, which is highest among the existing MRS devices in the literature. These devices will have high significance in futuristic "human-brain" like memory devices.

4. Experimental Section

PdO Thin Film Synthesis: Mica/quartz substrates were subsequently cleaned and ultrasonicated in water, Acetone and IPA, dried with

N_2 gas. A 100 µL of 50 m M Pd hexadecaylthiolate was drop-coated on the substrate at room temperature. The substrate was thermalized at 250 °C for 2 h in air following annealing at 600 °C for 3 h in oxygen atmosphere.

Characterization and Device Fabrication: The formed PdO thin film was well characterized before the device fabrication. A Perkin–Elmer Lambda 900 UV/visible/near-IR spectrophotometer was used to measure the absorption spectra of PdO thin film. XRD measurements on the PdO thin films were carried out using a Siemens Seifert 3000TT diffractometer (Cu Kα 1.5406 Å, scan rate, 1° min^{-1}). SEM and EDAX mapping was carried out using a Nova Nano SEM 600 instrument (FEI Co., The Netherlands). Raman measurements were performed using confocal Raman microscope (CRM-Alpha300 S), WITec GmbH, Germany. He-Ne laser with 633 nm wavelength was used. Raman maps were collected by stitching 2500 Raman spectra of PdO thin film over 6×6 µm^2 area. Electrical contacts were made by evaporating (Hind High Vacuum Co., India) Au using shadow mask of ≈7 µm on a 50 nm thick film. The electrical measurements were carried out on Keithley 4200 SCS and 236 source meter. Temperature dependent resistivity measurements were performed using THMS600 stage from Linkam Scientific Instruments Ltd, UK. The RS characteristics were measured in ambient at 21 °C and 35% RH.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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[1] G. I. Meijer, *Science* **2008**, *319*, 1625.
[2] R. Waser, M. Aono, *Nat. Mater.* **2007**, *6*, 833.
[3] Emerging Research Devices, Presented at *Int. Technol. Roadmap Semicond. (ITRS)* March 2013.
[4] B. Chen, X. Wang, B. Gao, Z. Fang, J. Kang, L. Liu, X. Liu, G.-Q. Lo, D.-L. Kwong, *Sci. Rep.* **2014**, *4*, 6863.
[5] J. Y. Seok, S. J. Song, J. H. Yoon, K. J. Yoon, T. H. Park, D. E. Kwon, H. Lim, G. H. Kim, D. S. Jeong, C. S. Hwang, *Adv. Funct. Mater.* **2014**, *24*, 5316.
[6] D. S. Jeong, R. Thomas, R. S. Katiyar, J. F. Scott, H. Kohlstedt, A. Petraru, C. S. Hwang, *Rep. Prog. Phys.* **2012**, *75*, 076502.
[7] A. Sawa, *Mater. Today* **2008**, *11*, 28.
[8] K. M. Kim, D. S. Jeong, C. S. Hwang, *Nanotechnology* **2011**, *22*, 254002.
[9] J. Ouyang, C.-W. Chu, C. R. Szmanda, L. Ma, Y. Yang, *Nat. Mater.* **2004**, *3*, 918.
[10] R. Waser, R. Dittmann, G. Staikov, K. Szot, *Adv. Mater.* **2009**, *21*, 2632.
[11] M. Liu, Z. Abid, W. Wang, X. He, Q. Liu, W. Guan, *Appl. Phys. Lett.* **2009**, *94*, 233106.
[12] S. K. Hwang, J. M. Lee, S. Kim, J. S. Park, H. I. Park, C. W. Ahn, K. J. Lee, T. Lee, S. O. Kim, *Nano Lett.* **2012**, *12*, 2217.
[13] Y. Guanwen, C. Hsiang-Yu, M. Liping, S. Yue, Y. Yang, *Appl. Phys. Lett.* **2009**, *95*, 203506.
[14] V. S. Reddy, S. Karak, A. Dhar, *Appl. Phys. Lett.* **2009**, *94*, 173304.
[15] Y. C. Yang, C. Chen, F. Zeng, F. Pan, *J. Appl. Phys.* **2010**, *107*, 093701.
[16] M. Lauters, B. McCarthy, D. Sarid, G. E. Jabbour, *Appl. Phys. Lett.* **2006**, *89*, 013507.
[17] C. Wu, F. Li, Y. Zhang, T. Guo, T. Chen, *Appl. Phys. Lett.* **2011**, *99*, 042108.
[18] T. Zhang, X. Zhang, L. Ding, W. Zhang, *Nanoscale Res. Lett.* **2009**, *4*, 1309.
[19] W. Yan, L. Qi, L. Shibing, W. Wei, W. Qin, Z. Manhong, Z. Sen, L. Yingtao, Z. Qingyun, Y. Jianhong, L. Ming, *Nanotechnology*, **2010**, *21*, 045202.
[20] R. Oligschlaeger, R. Waser, R. Meyer, S. Karthauser, R. Dittmann, *Appl. Phys. Lett.* **2006**, *88*, 042901.
[21] M. Colle, M. Buchel, D. M. de Leeuw, *Org. Electron.* **2006**, *7*, 305.
[22] C. Jiangshan, X. Liling, L. Jian, G. Yanhou, W. Lixiang, M. Dongge, *Semicond. Sci. Technol.* **2006**, *21*, 1121.
[23] J.-G. Park, W.-S. Nam, S.-H. Seo, Y.-G. Kim, Y.-H. Oh, G.-S. Lee, U.-G. Paik, *Nano Lett.* **2009**, *9*, 1713.
[24] Y. Zhang, J. X. Shen, S. L. Wang, W. Shen, C. Cui, P. G. Li, B. Y. Chen, W. H. Tang, *Appl. Phys. A: Mater.* **2012**, *109*, 219.
[25] L. Lifeng, G. Bin, C. Bing, Y. Chen, W. Yi, K. Jinfeng, H. Ruqi, presented at *10th IEEE Int. Conf. Solid-State Integr. Circuit Technol. (ICSICT)* November **2010**, Shanghai.
[26] W. Ming-Chi, J. Wen-Yueh, L. Chen-Hsi, T. Tseung-Yuen, *Semicond. Sci. Technol.*, **2012**, *27*, 065010.
[27] G. Ashvini, Y. Yee-Chia, *J. Appl. Phys.*, **2012**, *112*, 104504.
[28] M. Adnan, C. Sébastien, W. Maciej, H. Stephen, L. Christophe, R. Richard, J. K. Anthony, *Nanotechnology*, **2012**, *23*, 455201.
[29] H. K. Lau, C. W. Leung, *J. Appl. Phys.* **2008**, *104*, 123705.
[30] B. Hu, X. Zhu, X. Chen, L. Pan, S. Peng, Y. Wu, J. Shang, G. Liu, Q. Yan, R.-W. Li, *J. Am. Chem. Soc.*, **2012**, *134*, 17408.
[31] S.-C. Chen, T.-C. Chang, S.-Y. Chen, H.-W. Li, Y.-T. Tsai, C.-W. Chen, S. M. Sze, F.-S. Yeh, Y.-H. Tai, *Electrochem. Solid-State Lett.*, **2011**, *14*, H103.
[32] S.-J. Choi, G.-S. Park, K.-H. Kim, S. Cho, W.-Y. Yang, X.-S. Li, J.-H. Moon, K.-J. Lee, K. Kim, *Adv. Mater.*, **2011**, *23*, 3272.
[33] Y. Shimeng, W. Yi, H. S. P. Wong, *Appl. Phys. Lett.*, **2011**, *98*, 103514.
[34] B. Anirban, K. Miki, Y. Wakayama, *Appl. Phys. Lett.* **2006**, *89*, 243506.
[35] Y. Sharma, P. Misra, S. P. Pavunny, R. S. Katiyar, *Appl. Phys. Lett.* **2014**, *104*, 073501.
[36] C. He, Z. Shi, L. Zhang, W. Yang, R. Yang, D. Shi, G. Zhang, *ACS Nano*, **2012**, *6*, 4214.
[37] W. Sheng-Yu, H. Chin-Wen, L. Dai-Ying, T. Tseung-Yuen, C. Ting-Chang, *J. Appl. Phys.*, **2010**, *108*, 114110.
[38] Y. Chikako, T. Kohji, N. Hideyuki, S. Yoshihiro, *Appl. Phys. Lett.* **2007**, *91*, 223510.
[39] W. Yi, Y. Shimeng, H. S. P. Wong, C. Yu-Sheng, L. Heng-Yuan, W. Sum-Min, G. Pei-Yi, F. Chen, T. Ming-Jinn, presented at *4th IEEE Int. Memory Workshop (IMW)* May **2012**, Italy.
[40] Y. Jae Woo, H. Quanli, B. Yoon-Jae, C. Young Jin, K. Chi Jung, L. Hyun Ho, L. Do-Joong, K. Hyun-Mi, K. Ki-Bum, Y. Tae-Sik, *J. Phys. D: Appl. Phys.* **2012**, *45*, 225304.
[41] Y. C. Huang, P. Y. Chen, K. F. Huang, T. C. Chuang, H. H. Lin, T. S. Chin, R. S. Liu, Y. W. Lan, C. D. Chen, C. H. Lai, *NPG Asia Mater.* **2014**, *6*, e85.
[42] P.-H. Liu, C.-C. Lin, A. Manekkathodi, L.-J. Chen, *Nano Energy* **2015**, *15*, 362.
[43] H. Nili, S. Walia, A. E. Kandjani, R. Ramanathan, P. Gutruf, T. Ahmed, S. Balendhran, V. Bansal, D. B. Strukov, O. Kavehei, M. Bhaskaran, S. Sriram, *Adv. Funct. Mater.* **2015**, *25*, 3172.
[44] L. Zhao, H. Y. Chen, S. C. Wu, Z. Jiang, S. Yu, T. H. Hou, H. S. P. Wong, Y. Nishi, *Nanoscale* **2014**, *6*, 5698.

[45] K. Oka, T. Yanagida, K. Nagashima, T. Kawai, J.-S. Kim, B. H. Park, *J. Am. Chem. Soc.* **2010**, *132*, 6634.
[46] S. Gao, C. Chen, Z. Zhai, H. Y. Liu, Y. S. Lin, S. Z. Li, S. H. Lu, G. Y. Wang, C. Song, F. Zeng, F. Pan, *Appl. Phys. Lett.* **2014**, *105*, 063504.
[47] J. Qi, M. Olmedo, J. Ren, N. Zhan, J. Zhao, J.-G. Zheng, J. Liu, *ACS Nano* **2012**, *6*, 1051.
[48] S. Yu, H.-Y. Chen, B. Gao, J. Kang, H. S. P. Wong, *ACS Nano* **2013**, *7*, 2320.
[49] Y. Bai, H. Wu, R. Wu, Y. Zhang, N. Deng, Z. Yu, H. Qian, *Sci. Rep.* **2014**, *4*, 5780.
[50] R. Westerström, M. E. Messing, S. Blomberg, A. Hellman, H. Grönbeck, J. Gustafson, N. M. Martin, O. Balmes, R. van Rijn, J. N. Andersen, K. Deppert, H. Bluhm, Z. Liu, M. E. Grass, M. Hävecker, E. Lundgren, *Phys. Rev. B* **2011**, *83*, 115440.
[51] Y.-J. Chiang, K.-C. Li, Y.-C. Lin, F.-M. Pan, *Phys. Chem. Chem. Phys.* **2015**, *17*, 3039.
[52] D. Yu, C. Wang, B. L. Wehrenberg, P. Guyot-Sionnest, *Phys. Rev. Lett.* **2004**, *92*, 216802.
[53] A. Baylet, P. Marecot, D. Duprez, P. Castellazzi, G. Groppi, P. Forzatti, *Phys. Chem. Chem. Phys.* **2011**, *13*, 4607.
[54] J. Han, *Ph.D. Thesis*, Worcester Polytechnic Institute, **2004**.
[55] K. Mølhave, S. B. Gudnason, A. T. Pedersen, C. H. Clausen, A. Horsewell, P. Bøggild, *Nano Lett.* **2006**, *6*, 1663.
[56] J. R. McBride, K. C. Hass, W. H. Weber, *Phys. Rev. B* **1991**, *44*, 5016.
[57] C. B. Lee, B. S. Kang, M. J. Lee, S. E. Ahn, G. Stefanovich, W. X. Xianyu, K. H. Kim, J. H. Hur, H. X. Yin, Y. Park, I. K. Yoo, J.-B. Park, B. H. Park, *Appl. Phys. Lett.* **2007**, *91*, 082104.
[58] G. Ketteler, D. F. Ogletree, H. Bluhm, H. Liu, E. L. D. Hebenstreit, M. Salmeron, *J. Am. Chem. Soc.* **2005**, *127*, 18269.

